NATIONAL UNIVERSITY OF SCIENCE AND TECHNOLOGY POLITEHNICA BUCHAREST

Doctoral School of Electronics, Telecommunications and Information Technology

Ph.D. THESIS SUMMARY

Ionuț-Constantin GURAN

CONTRIBUȚII ÎN MANAGEMENTUL BATERIILOR DIN DOMENIUL AUTO

CONTRIBUTIONS IN AUTOMOTIVE BATTERY MANAGEMENT

THESIS COMMITTEE

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BUCHAREST 2025

Content

Chapter 1

Introduction

As the world shifts towards greener energy, batteries play a key role in modern automotive and Energy Storage Systems (ESS). A major challenge is the disparity in State of Charge (SOC) among individual cells, which reduces battery lifespan. Advanced Battery Management Systems (BMS) address this issue by using SOC estimation and balancing techniques to ensure cells operate harmoniously, enhancing battery performance and longevity. BMS also acts to prevent damage and maintain performance during anomalies. In the fast-paced electronics industry, engineers use simulation, particularly Simulation Program ofr Integrated Circuits Emphasis (SPICE), to develop and validate circuit designs quickly, ensuring optimal performance before physical implementation.

1.1 Presentation of the field of the doctoral thesis

Lithium Iron Phosphate (LiFePO4) batteries have become a preferred choice for the automotive industry due to their low self-discharge rates, high energy density, efficiency, longer cycle lifetimes, and improved safety. Despite these advantages, their capacity decreases over time, requiring replacement when it falls below 80% of the nominal capacity. Continuous monitoring of the State of Health (SOH) and SOC is essential for optimal performance. The BMSs help mitigate degradation by monitoring key parameters and initiating cell equalization when necessary. Simulation, particularly using SPICE, is essential for designing and verifying these systems, allowing for early issue identification and cost-effective development.

This doctoral thesis focuses on creating a full SPICE model for a passive BMS for the first time in the domain literature, along with the design of a passive BMS that has superior performances compared with other similar circuits proposed until now. Chapter 1 presents the field of the doctoral thesis, the scope of the doctoral thesis, and its content. The proposed doctoral thesis treats the LiFePO4 batteries and battery management systems field, including the design, SPICE simulation, implementation and verification of such circuits, illustrating at the same time the complete cycle an engineer has to follow when creating a circuit or system.

1.2 Scope of the doctoral thesis

Recent literature has shown high interest in BMSs for ensuring the reliability and efficiency of battery-powered systems, especially through cell balancing techniques. Passive cell balancing dissipates excess energy from overcharged cells, while active balancing transfers energy between cells to maintain balance. Passive balancing is favored for its simplicity, lower cost, and ease of implementation. Modern BMS also rely on remote monitoring for real-time performance insights, yet the full benefits of this feature are underexplored. Additionally, while physical design and verification of BMS are well-studied, comprehensive SPICE simulation models are rare. This doctoral thesis aims to develop a complete SPICE model for BMS designed for LiFePO4 cells and implement a fast balancing passive BMS with remote monitoring, tailored for the automotive industry, to enhance the safety and performance of these systems.

1.3 Content of the doctoral thesis

This PhD thesis presents the process an engineer must follow to develop a full SPICE model of a Battery Management System (BMS), a novelty in the literature, alongside the design and physical implementation of an improved BMS.

- **Chapter 2** synthesizes existing BMS research, highlighting key findings and limitations, and sets the stage for this thesis's innovations.
- **Chapter 3** details the development of a SPICE simulation model for LiFePO4 cells, comparing their performance with other Li-ion chemistries and verifying the detailed cell model.
- **Chapter 4** introduces an innovative methodology for modeling the On-State Resistance (RDS_{ON}) of Metal Oxide Semiconductor Field Effect Transistor (MOSFET) power switches, showing benefits over existing models.
- **Chapter 5** proposes a novel approach to modeling the Power Supply Rejection Ratio (PSRR) in automotive Low Drop Out (LDO) voltage regulators, modifying an existing model to accommodate new PSRR behavior.
- **Chapter 6** focuses on creating SPICE models for digital circuits used in BMS, improving understanding and reliability of the BMS's internal architecture.
- **Chapter 7** develops a full SPICE model for a BMS that balances four LiFePO4 cells, incorporating cell voltage sensing, balancing, current monitoring, power supply, and an emulated Microcontroller (MCU).
- **Chapter 8** covers the hardware development and integration of a passive BMS with remote monitoring for automotive platforms, demonstrating superior performance compared to existing systems.

Chapter 2

Literature Survey

To develop more efficient, reliable, and sustainable BMSs, it is essential to build on previous research. This chapter comprehensively reviews existing studies in the BMS domain, analyzing their findings and limitations to identify areas for improvement and opportunities for innovation. This analysis lays the groundwork for the advancements presented in this thesis, which aim to address the gaps in current BMS design, simulation, and implementation. Understanding the current state of BMS research enables the creation of innovative solutions with significant industry impact.

2.1 Literature survey on BMS design

In 2021, Wu et al. introduced a BMS for Electric Vehicles (EVs) using the LTC6811 monitor and NuMicro M487 microcontroller without prior simulation, limiting its validation [14].

In 2022, Liu et al. [15] developed a BMS for Electronic Management Units (EMUs) storage systems with a master-slave architecture, validated only for SOC estimation in Matlab.

Prakasha et al.'s [16] 2022 BMS for EVs featured a master-slave setup with Raspberry Pi and Arduino, using a constant current load for cell balancing but lacked prior simulation. Similarly, Ding et al. [17] proposed an active flyback Direct Current – Alternating Current (DC-AC) balancing BMS for larger packs, also without simulation.

Rehman et al. [18] presented an Internet of Things (IoT)-based BMS for EVs focusing on monitoring but missed cell balancing and simulation. Gullu et al. [19] designed a high-voltage BMS for PhotoVoltaic (PV) systems, validating only a Direct Current – Direct Current (DC-DC) converter in simulations.

Lastly, in 2021, Guran et al. [20] introduced an automotive BMS with some components validated in LTSpice, but a full model was suggested for future work.

2.2 Literature survey on BMS cell balancing techniques

Pattnaik et al. (2023) [11] developed a novel BMS design that alerts users to faults and balances the SOC during charging. They simulated passive, active, and lossless balancing techniques, noting that active balancing offers faster times and higher efficiency compared to passive balancing, which is simpler and cheaper.

Nath and Rajpathak (2022) [21] compared passive and active balancing techniques in BMSs for electric vehicles, finding that passive balancing is simpler but less efficient, while active balancing reduces charge losses but is more complex and costly. Kumar et al. (2022) [22] conducted a theoretical comparison of passive and active balancing methods, emphasizing the trade-offs between cost, efficiency, and complexity. They concluded that no single method is optimal for all applications, necessitating careful consideration of specific requirements.

Karmakar et al. (2023) [23] introduced a BMS design using a Proportional-Integral-Derivative (PID) controller with passive balancing, demonstrating improved precision and reduced balancing time, though they did not explore remote monitoring capabilities. Dalvi and Thale (2020) [24] presented a Digital Signal Processor (DSP)-controlled BMS with passive balancing for Evs and Hybrid Electric Vehicles (HEVs), highlighting its reliability and simplicity. They noted the potential for enhanced performance with remote monitoring features.

2.3 Conclusions of chapter 2

The literature surveys in sections 2.1 and 2.2, *also published in author's research articles [26] and [27]*, highlight several key points.

Section 2.1 reveals significant research attention on the physical design and verification of BMS, noting a gap in the development of a full-functionality BMS SPICE model. Such a model is important for creating physical BMS prototypes, reducing development time and costs, and ensuring fault-free final products.

Section 2.2 emphasizes the importance of BMS in automotive and energy storage, comparing active and passive cell balancing techniques. Active balancing offers rapid times and high efficiency but is complex and costly, while passive balancing is simpler, more compact, and cost-effective despite lower efficiency and slower processes. The literature favors passive balancing for HEVs and EVs. Additionally, remote monitoring of battery parameters is identified as an important but under-researched aspect in modern BMS.

Chapter 3

Simulation Model for LiFePO4 Cell

3.1 LiFePO4 cell model importance

Lithium batteries, especially LiFePO4, are preferred for energy storage due to their high power densities and long lifespan. LiFePO4 batteries offer excellent electrochemical performance, low internal resistance, good thermal stability, and high safety features.

However, their performance can be affected by temperature extremes. Designing battery-powered circuits requires simulating both the battery and the circuit to ensure reliability and prevent damage. The following subchapters propose a SPICE model for a China Aviation Lithium Battery (CALB) CA180FA LiFePO4 battery cell, focusing on key characteristics to provide an accurate representation of its behavior [30].

3.2 LiFePO4 cell model implementation

The analog behavioral model of the cell is graphically represented in Figure 3.3, which illustrates the incorporation of the Open Circuit Voltage (OCV) = f(SOC) characteristic of the LiFePO4 cell, as well as its internal resistance, into the model.

```
.SUBCKT LIFEPO4_CELL  CEL+  CEL-  SOC  PARAMS:
+ NOMINAL_CAPACITY = 180
+ INTERNAL_RESISTANCE = 0.6m
+ INITIAL_SOC = 1

E_OCV       CELP   CELN  TABLE {V(SOC)} =
+ (0, 2.5)       (0.03, 2.8)    (0.05, 2.9)
+ (0.075, 3)     (0.1, 3.1)     (0.12, 3.17)
+ (0.2, 3.2)     (0.3, 3.23)    (0.4, 3.28)
+ (0.5, 3.29)    (0.6, 3.3)     (0.65, 3.3)
+ (0.7, 3.31)    (0.76, 3.32)   (0.8,3.33)
+ (0.9,3.34)     (0.95,3.35)    (0.97 ,3.37)
+ (0.98,3.38)    (1, 3.5)

V_CSENSE    CELN   CEL-
R_INT       CELP   CEL+   {INTERNAL_RESISTANCE}
R_CONV      CEL+   CEL-   1e12


CCELL_CAPACITY       SOC     0     {3600 * NOMINAL_CAPACITY}
GBAT_CURRENT         0       SOC   VALUE={I(V_CSENSE) * IF(V(SOC) < 0
+& I(V_CSENSE) <0  ,0,1) * IF(V(SOC) > 1 & I(V_CSENSE) > 0,0,1) }
RSOC                 SOC     0     1e12

.IC V(SOC)={INITIAL_SOC}

.ENDS
```

Figure 3.3 *SPICE model implementation of the LiFePO4 cell*

3.3 LiFePO4 cell model testing

The OCV = f(SOC) characteristic of the proposed SPICE model for the LiFePO4 cell, as obtained through simulation, is illustrated in Figure 3.5.

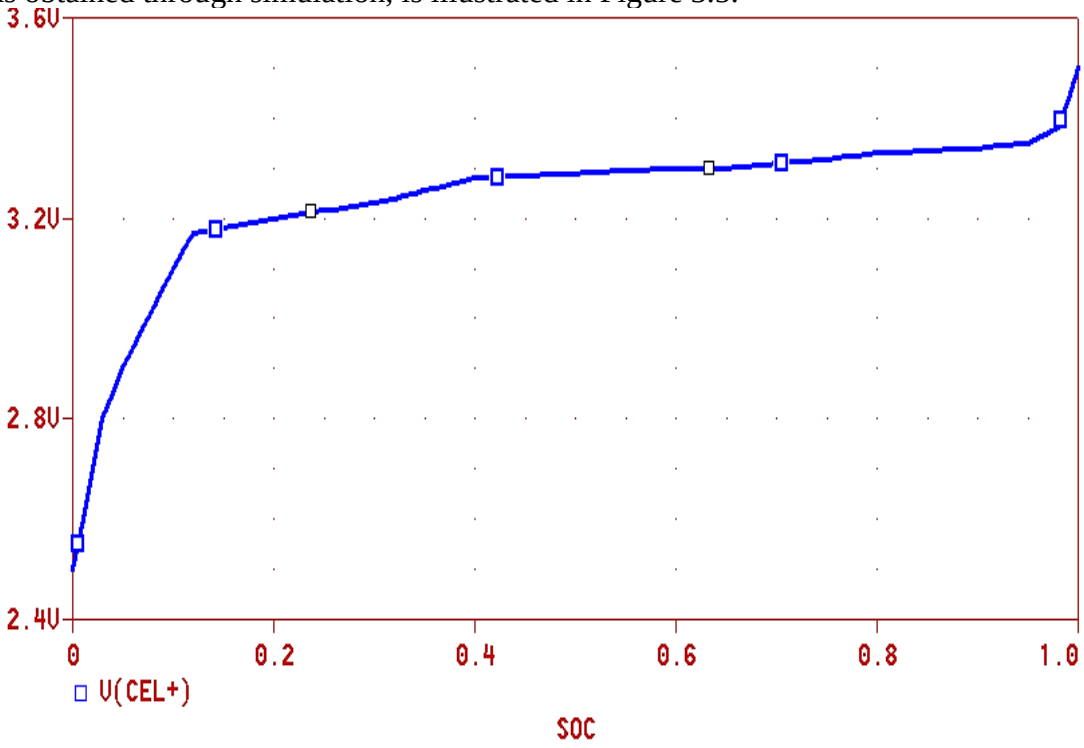


Figure 3.5 *Simulated OCV = f(SOC) characteristic of the proposed model*

3.4 Conclusions of chapter 3

This chapter, *based on one of the author's research papers [30]*, presents a novel SPICE model for a CALB CA180FA LiFePO4 battery cell. This model, compatible with various simulation software like OrCAD Capture CIS, Pspice Allegro, TINA, SIMetrix, and LTSpice, enables accurate simulation of advanced energy storage systems, battery management systems, and other battery-powered circuits. The model accurately replicates the OCV-SOC relationship and internal resistance of the CALB LiFePO4 cell, demonstrating high accuracy, fast simulation speeds, and reliable convergence in transient behavior.

Chapter 4

Innovative Approach to Modeling ON-State Resistance in MOSFET Power Switches

4.1 Background and context

Accurate simulation using tools like PSpice is important, with RDS_{ON} being an important MOSFET parameter affected by temperature and gate voltage. Existing models have limitations in capturing RDS_{ON} variation over temperature. This chapter proposes a novel RDS_{ON} modeling method for MOSFETs, enabling precise simulation over the entire operating range.

4.2 Texas Instruments' CSD13380F3 MOSFET model: Simulation-based performance evaluation

The CSD13380F3 N-channel MOSFET from Texas Instruments is versatile, featuring a low RDS_{ON}, high operating drain current, and a compact footprint. Texas Instruments also provides a SPICE simulation model for CSD13380F3.

Figure 4.10 illustrates the simulated RDS_{ON} versus V_{GS} characteristics for the CSD13380F3 model.

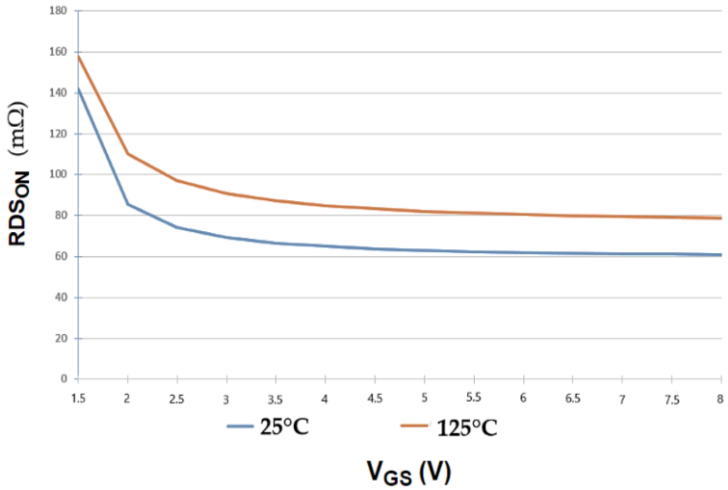


Figure 4.10 *Simulated RDS_{ON} vs. V_{GS} for Texas Instruments' CSD13380F3 model*

Figure 4.12 displays the normalized RDS_{ON} versus T_C behavior for the Texas Instruments CSD13380F3 MOSFET model.

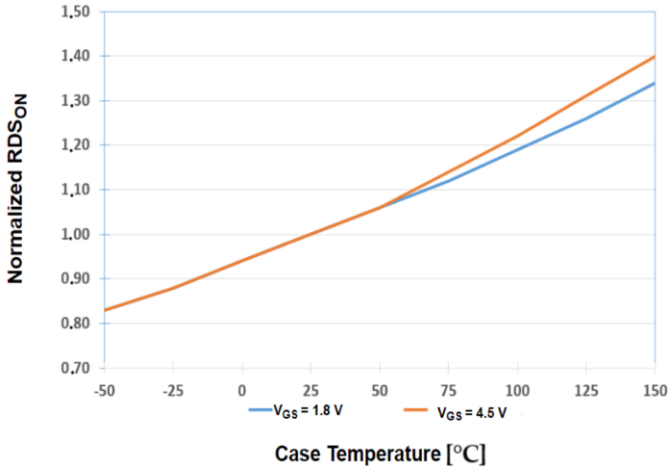


Figure 4.12 *Simulated RDS_{ON} vs. T_C for Texas Instruments' CSD13380F3 model*

4.3 Approach and procedures for the new CSD13380F3 MOSFET model

Figure 4.13 illustrates the innovative principle for modeling ON-state resistance RDS_{ON}.

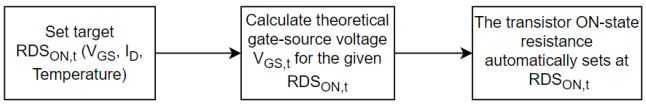


Figure 4.13 *Novel modeling principle of the RDS_{ON}*

4.4 Simulation results for the novel proposed CSD13380F3 MOSFET model

The simulated characteristic of RDS_{ON} versus V_{GS} for the newly developed CSD13380F3 model is illustrated in Figure 4.17.

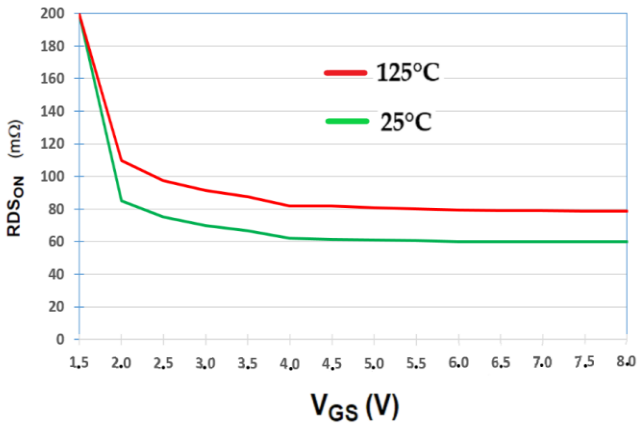


Figure 4.17 *RDS_{ON} vs. V_{GS} waveforms for the novel CSD13380F3 model*

The graph in Figure 4.19 illustrates the normalized RDS_{ON} versus T_C characteristic of the newly developed CSD13380F3 MOSFET model.

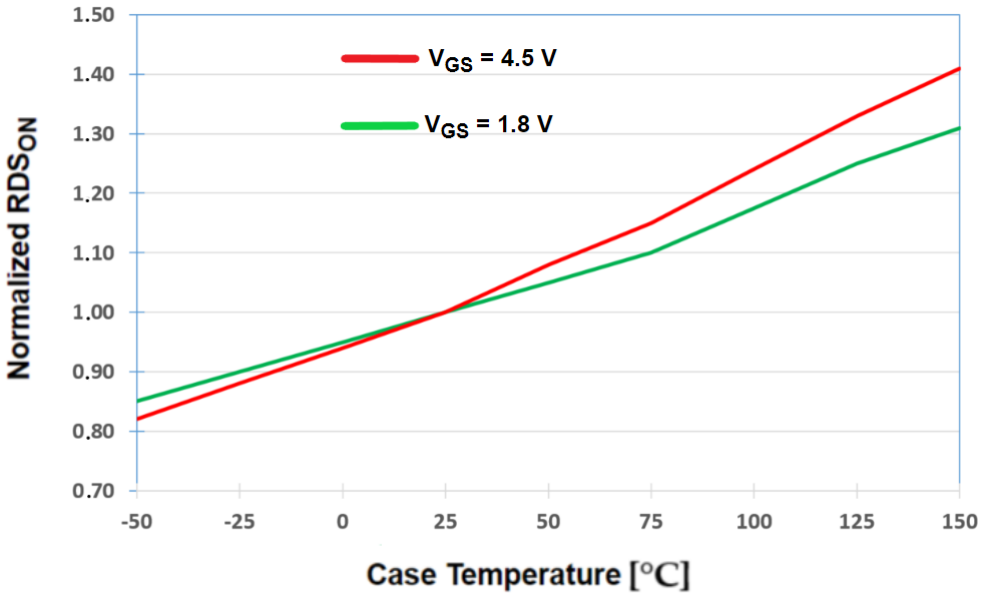


Figure 4.19 *Simulated normalized RDS_{ON} vs. T_C characteristics for the novel CSD13380F3 model*

4.5 Discussion and comparison

The calculated relative deviation from the theoretical characteristic of the Texas Instruments' model ($RDS_{ON,TI}$ Error) ranges from 0.08% to 29.12%. In contrast, the new model exhibits a significantly improved accuracy, with a relative error ($RDS_{ON,New}$ Error) spanning from 0% to 0.08.

The normalized RDS_{ON} relative error for the Texas Instruments' model (Normalized $RDS_{ON,TI}$ Error) ranges from 0% to 2.35%, whereas the normalized RDS_{ON} relative error for the new model (Normalized $RDS_{ON,New}$ Error) falls between 0% and 0.8%.

4.6 Conclusions of chapter 4

The research shown in this chapter, *which was also presented in one of author's previous research papers [68]*, highlights a groundbreaking approach to modeling ON-state resistance in MOSFET power switches. The proposed technique involves dynamically adjusting the gate-source voltage of the MOSFET to achieve a specific target RDS_{ON} value, thereby enabling precise control over the device's ON-state resistance. By modulating the gate-source voltage, the method allows for the optimization of RDS_{ON}, a parameter that significantly impacts the overall performance and efficiency of power electronic systems.

Chapter 5

Enhanced Simulation Framework for Automotive LDO Voltage Regulators: A Novel Approach to PSRR Modeling

Simulation is key in automotive design for validating systems and identifying faults. Accurate models are needed for components like LDOs, which power subsystems. Existing LDO models capture many characteristics, but PSRR modeling is challenging. This chapter introduces a novel PSRR modeling technique for automotive LDOs, applied to a Texas Instruments product and simulated with PSpice Allegro and OrCAD Capture CIS.

5.1 Context and motivation

Existing research on PSRR focuses on physical design, lacking in simulation modeling. This chapter addresses this gap by proposing an innovative approach to optimizing PSRR modeling in the simulation domain, with a particular emphasis on achieving high accuracy for automotive LDO voltage regulators.

5.2 Understanding LDO PSRR: A review of the fundamentals

In the fields of power electronics and automotive systems, the PSRR is a major parameter. The PSRR characteristic of a specific automotive high PSRR LDO regulator, TPS785-Q1, is illustrated in Figure 5.4. Texas Instruments also provides a simulation model for TPS785-Q1.

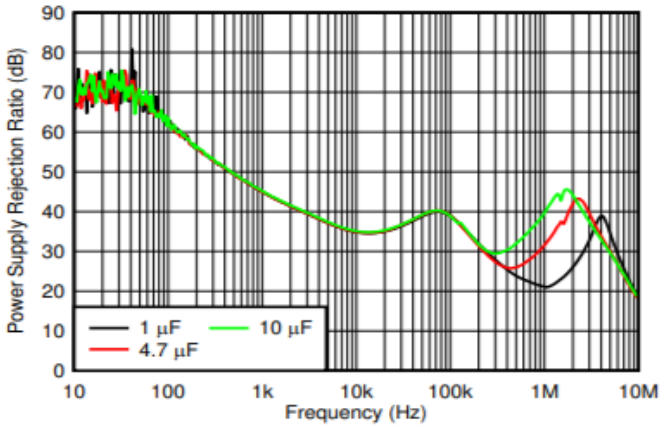


Figure 5.4 *C_{OUT} influence over PSRR at V_{OUT} = 3.3 V and I_{OUT} =1 A*

The simulated PSRR characteristics of the TPS785-Q1 LDO model provided by Texas Instruments, plotted as a function of frequency, are presented in Figure 5.9.

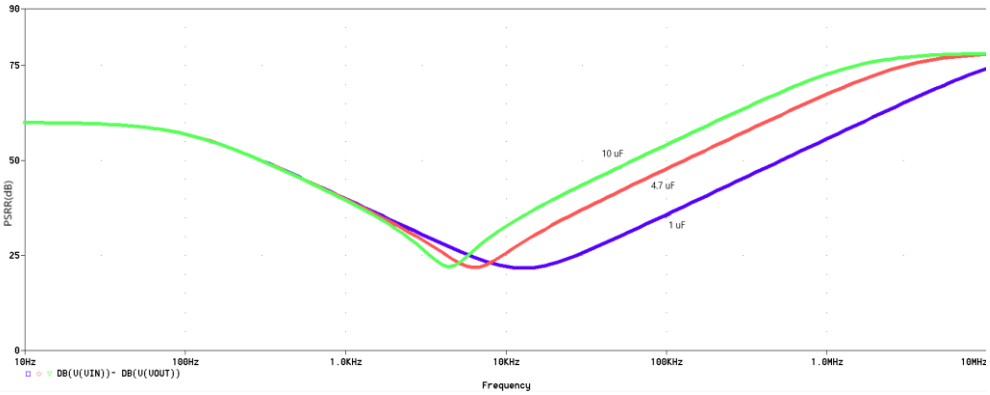


Figure 5.9 *Simulated PSRR characteristic of the initial TPS785-Q1 model*

5.3 Development and implementation of the novel PSRR model: Materials and methods

The existing TPS785-Q1 model from Texas Instruments was updated by removing the outdated PSRR characteristic and incorporating a new PSRR concept shown in Figure 5.10.

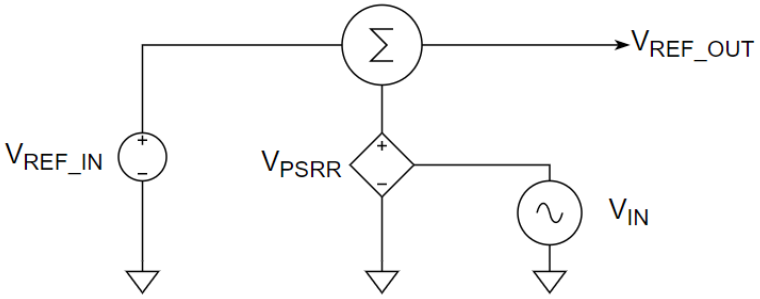


Figure 5.10 *Concept diagram of the novel LDO PSRR model*

5.4 Simulated performance of the novel PSRR model

The new frequency-dependent PSRR is shown in Figure 5.16.

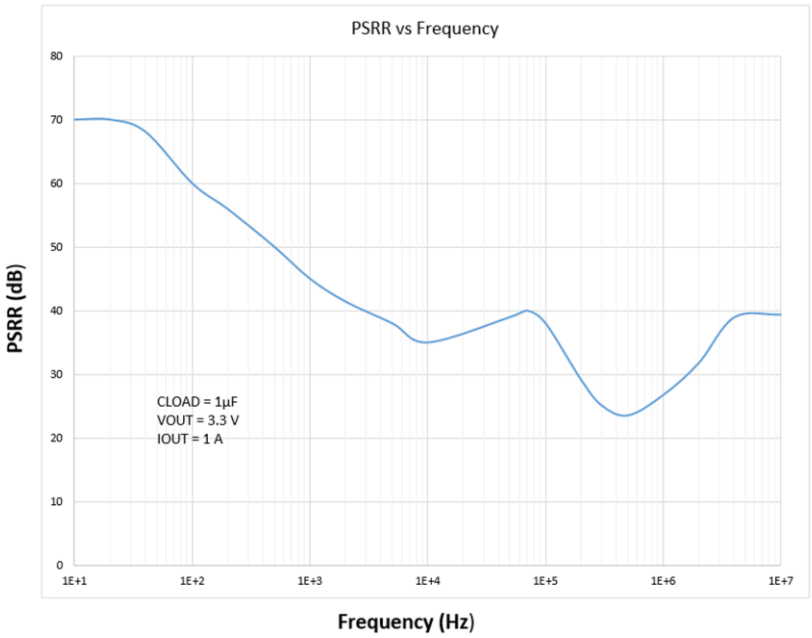


Figure 5.16 *Frequency response of the new TPS785-Q1 PSRR model performance*

5.5 Analyzing and contrasting theoretical and simulated PSRR results: A comparative study

The new PSRR approach performs better at frequencies below 500 kHz, with a relative error of 0% to 7%, compared to the conventional model's 5% to 100% error. Both models exhibit higher error rates above 500 kHz due to limitations of the error amplifier, which needs redesigning for better high-frequency PSRR performance.

5.6 Conclusions of chapter 5

This chapter introduces a novel approach to enhance the PSRR response of automotive LDO models at frequencies below 500 kHz, using mathematical correlations and circuit relationships. *This concept was initially presented in one of author's earlier research articles [93].*

Based on the TPS785-Q1 model from Texas Instruments, a new non-linear PSRR model was developed and integrated. Transient simulations showed excellent behavior below 500 kHz with less than 7% error, but inaccuracies above 500 kHz due to the error amplifier. Accurate LDO models are important for automotive simulations, yet most lack precise PSRR characterization. This chapter fills this gap by presenting an optimized PSRR model and suggesting future research on error amplifier redesign for higher frequencies.

Chapter 6

Digital Circuit Modeling Approaches in BMS Design

6.1 Digital up-counter design for BMS: A SPICE-based implementation

Digital counters are important in digital and mixed signal systems, including BMS. Accurate behavioral models for these counters are needed for effective BMS modeling. This subchapter presents a novel SPICE-based implementation of a digital up-counter for BMS, featuring a four-bit output up-counter.

The SPICE model of the four-bit digital counter in shown in Figure 6.2.

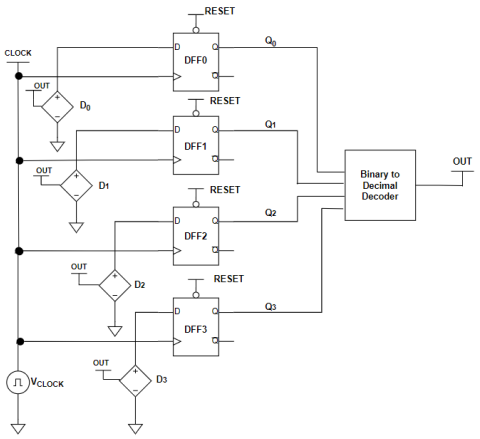


Figure 6.2 *Operating mechanism of the 4-bit up-counter*

Figure 6.6 shows only the simulation results of the counter operating at a 100 kHz clock frequency.

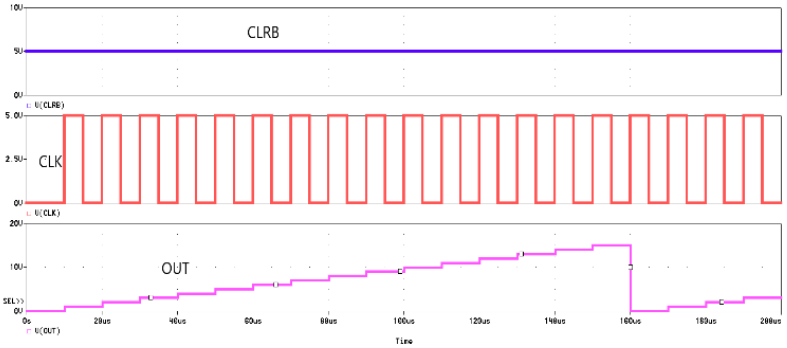


Figure 6.6 *Simulation results for normal operation of the up-counter at 100 kHz*

A novel SPICE implementation of digital up-counters for BMSs, using D flip-flops and binary to decimal conversion, is proposed. The model focuses on a four-bit counter with three pins: CLK (input clock), CLRB (reset signal), and OUT (decimal output). *This model was detailed in a previous research paper by the author [119]*.

6.2 Enhanced countdown functionality in SPICE

Counting operations are important in digital circuits. Most research focuses on four-bit up-down counters. This subchapter introduces a SPICE model for down-counters, eliminating output size limits and enabling fast simulations. The model is validated with OrCAD Capture and tested across 1 kHz to 1 GHz.

The advanced down-counter model eliminates output size limits and enables fast simulations. Figure 6.10 shows its schematic with four pins: OUT (output), STARTING_VALUE (initial value), CLK (clock signal), and RESET (resets to STARTING_VALUE).

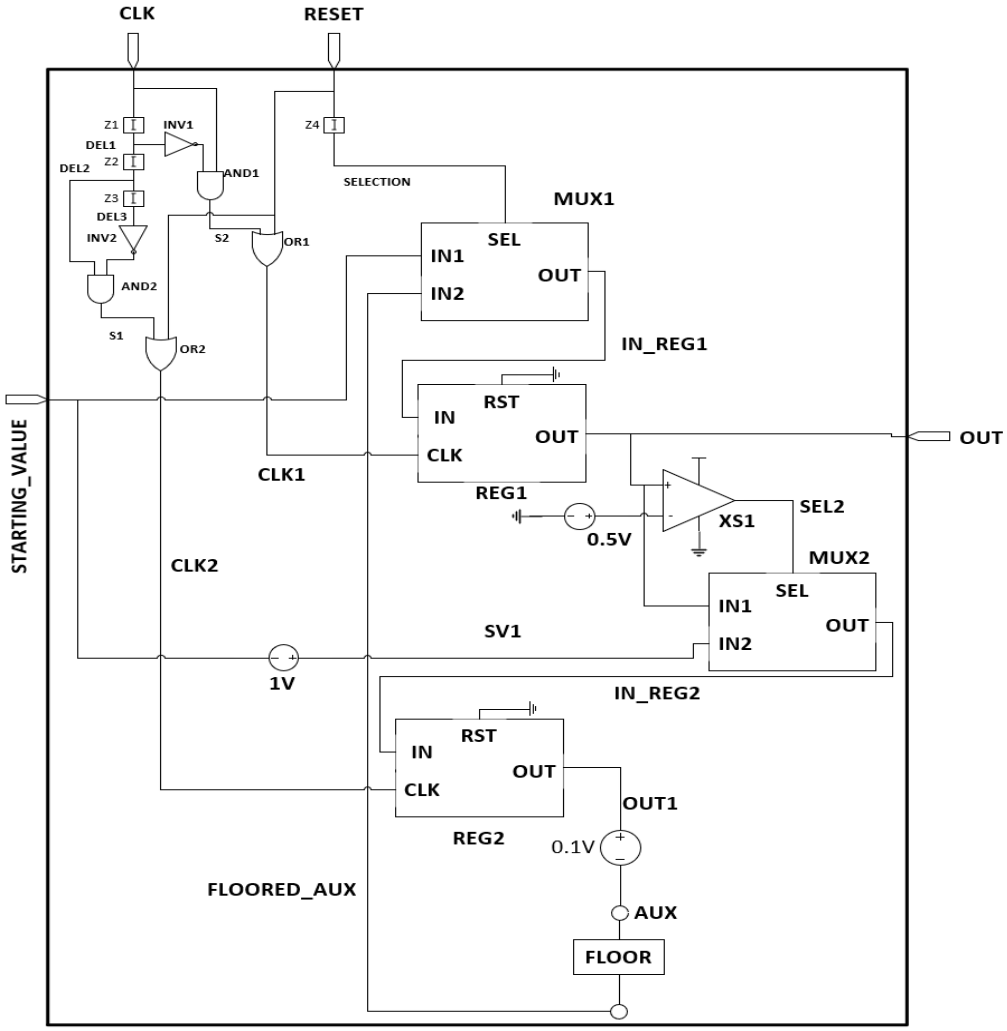


Figure 6.10 *Block diagram of the proposed down-counter SPICE model*

Figure 6.14 shows only the 1 MHz clock waveforms..

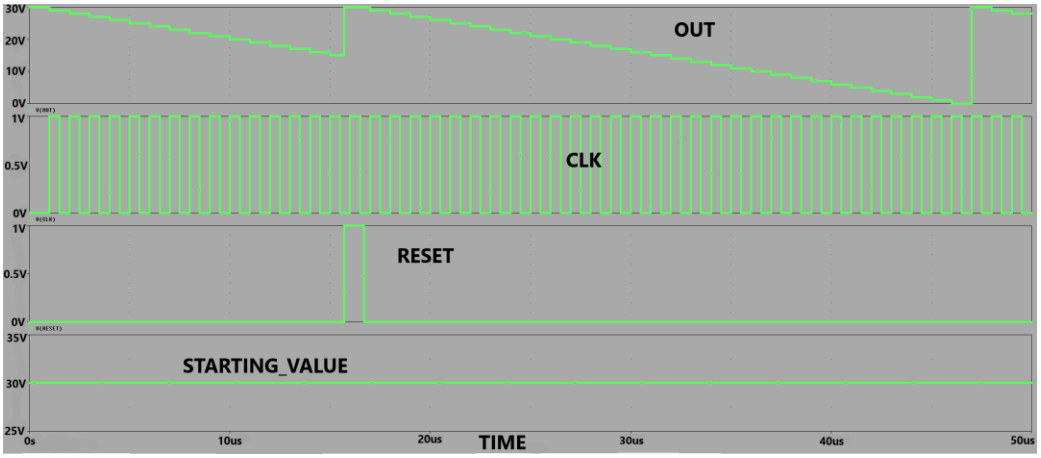


Figure 6.14 *Down-counting operation waveforms at a clock frequency of 1 MHz*

Subchapter 6.2 introduced a SPICE down-counter model that decrements from any user-defined value and can be reset anytime. *A previous publication by the author detailed this model [120]*. It overcomes output size limits using a feedback loop, analog-output registers, and multiplexers. Verified with OrCAD Capture from 1 kHz to 1 GHz, the counter operates correctly.

6.3 Clock signal generation for SPICE-based simulation environments

Subchapter 6.3 introduces a novel approach to generating high-precision clock signals in analog form, compatible with all SPICE-based simulators like PSpice Allegro, SIMetrix, TINA, and LTSpice. This method addresses the challenge of differing simulator characteristics and lack of a common language, particularly for digital circuits.

Figure 6.16 shows the fully analog clock signal generator.

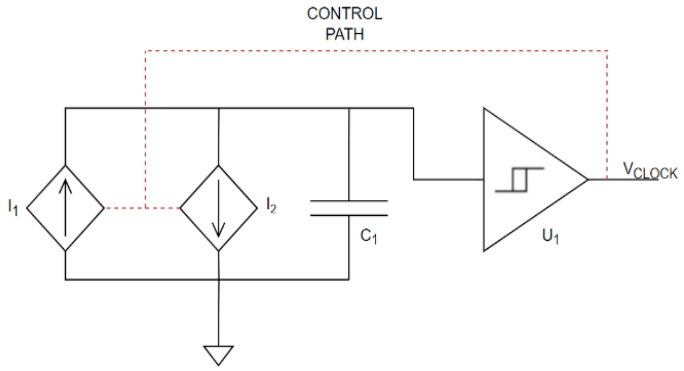


Figure 6.16 *Clock signal generator principle of operation*

Figure 6.19 presents a graphical representation of the clock signal waveform in OrCAD Capture CIS, with a chosen switching frequency of 4 MHz for demonstration purposes.

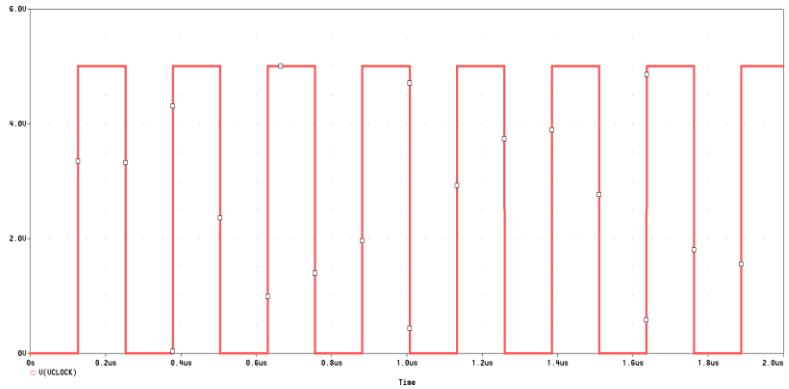


Figure 6.19 *Simulation waveform at 4 MHz in OrCAD Capture CIS*

The clock frequency error range observed is between 0.07% and 3.55%, with the maximum deviation occurring at a frequency of 20 MHz.

Subchapter 6.3 presented a novel analog clock signal generator for SPICE-based simulators. Compatible with OrCAD Capture CIS, SIMetrix, TINA, and LTSpice, *the model was detailed in an author's previous paper [121]*.

6.4 Enhanced slew rate control methodology in SPICE for automotive LDO models

Subchapter 6.4 presents an optimized slew rate control technique for automotive LDO models, usable in BMS modeling. This technique was integrated into the TPS7B88-Q1 LDO model and tested with OrCAD Capture CIS.

Figure 6.28 illustrates the TPS7B88-Q1 LDO's start-up timing with 150 mA output current and 10 µF capacitor. Measured between 10% and 90% of the final voltage, the theoretical slew rate ($SR_{theoretical}$) is 25 V/ms.

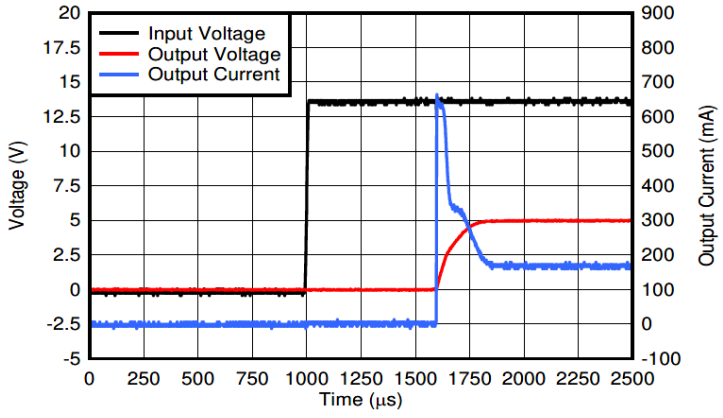


Figure 6.28 *TPS7B88-Q1 start-up timing*

Figure 6.30 shows the start-up behavior of the TPS7B88-Q1 model provided by Texas Instruments. Measuring between 10% (0.5 V) and 90% (4.5 V) of the final value, the simulated slew rate ($SR_{initial,\ simulated}$) is 12.37 V/ms, with an error ($ERR_{initial,\ simulated}$) of 50.52% compared to the theoretical 25 V/ms.

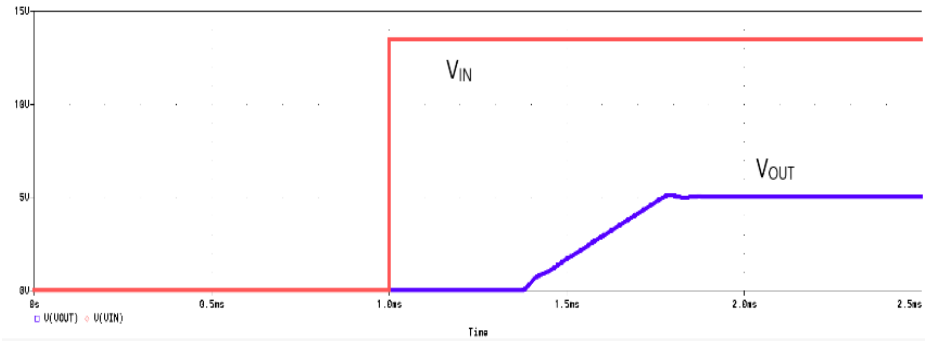


Figure 6.30 *Baseline TPS7B88-Q1 model start-up waveforms*

Figure 6.31 shows the optimized slew rate control technique principle.

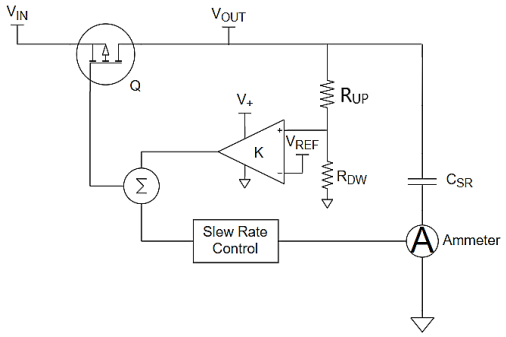


Figure 6.31 *Diagram of the novel LDO model with enhanced SR functionality*

Figure 6.34 shows the LDO's start-up with the new slew rate control technique. The new slew rate is 25.48 V/ms, with a 1.92% error from the 25 V/ms target.

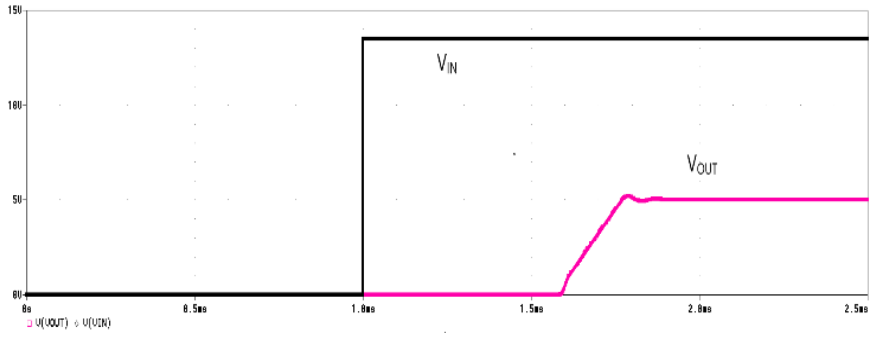


Figure 6.34 *Novel TPS7B88-Q1 model start-up diagram*

Subchapter 6.4 presented an optimized slew rate control methodology for automotive LDO regulators based on the capacitor principle, *previously detailed in the author's research paper [142]*. The method was validated using the TPS7B88-Q1 LDO regulator from Texas Instruments, available in an unencrypted format on the manufacturer's website.

Simulations were conducted using OrCAD Capture CIS. The initial unmodified model showed a slew rate of 12.37 V/ms with a 50.52% error. After reverse engineering and adding the novel slew rate controller, the improved model achieved a slew rate of 25.48 V/ms, with a 1.92% error.

6.5 An innovative technique for measuring frequency in SPICE simulations: Enhancing clock synchronization accuracy

Existing research focuses on physical frequency measurement, ignoring SPICE simulations. Commercial SPICE simulators measure frequency post-simulation, limiting real-time synchronization. This subchapter introduces a new method for real-time clock synchronization in SPICE-based simulators.

The single clock period measurement subcircuit samples a single clock period and is part of the clock frequency measurement block.

The MULTIPLE_CLOCK_PERIOD_MEAS subcircuit in Figure 6.41 measures multiple clock periods using two SINGLE_CLOCK_PERIOD_MEAS instances (XODD and XEVEN).

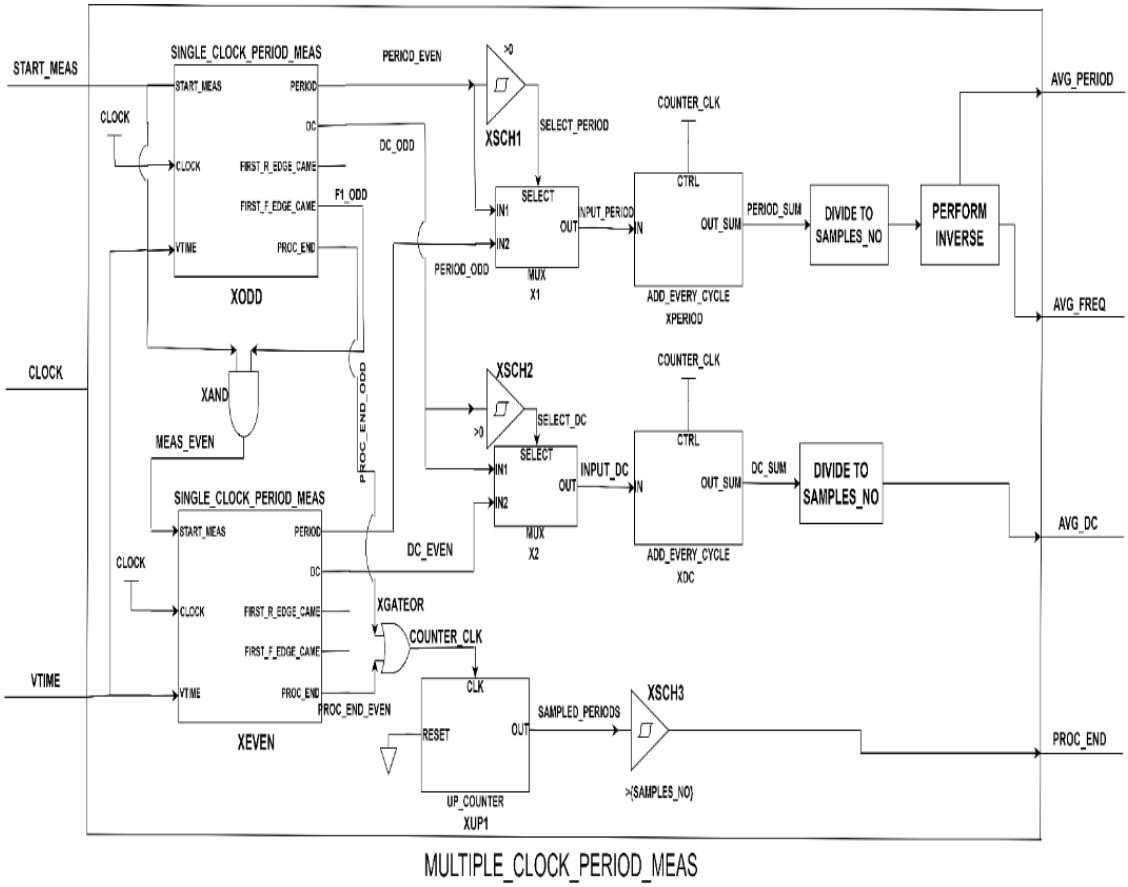


Figure 6.41 *SPICE schematic of the MULTIPLE_CLOCK_PERIOD_MEAS subcircuit*

Figure 6.48 shows the waveforms for a 10 kHz clock frequency, 0.2 duty cycle, and SAMPLES_NO = 100.

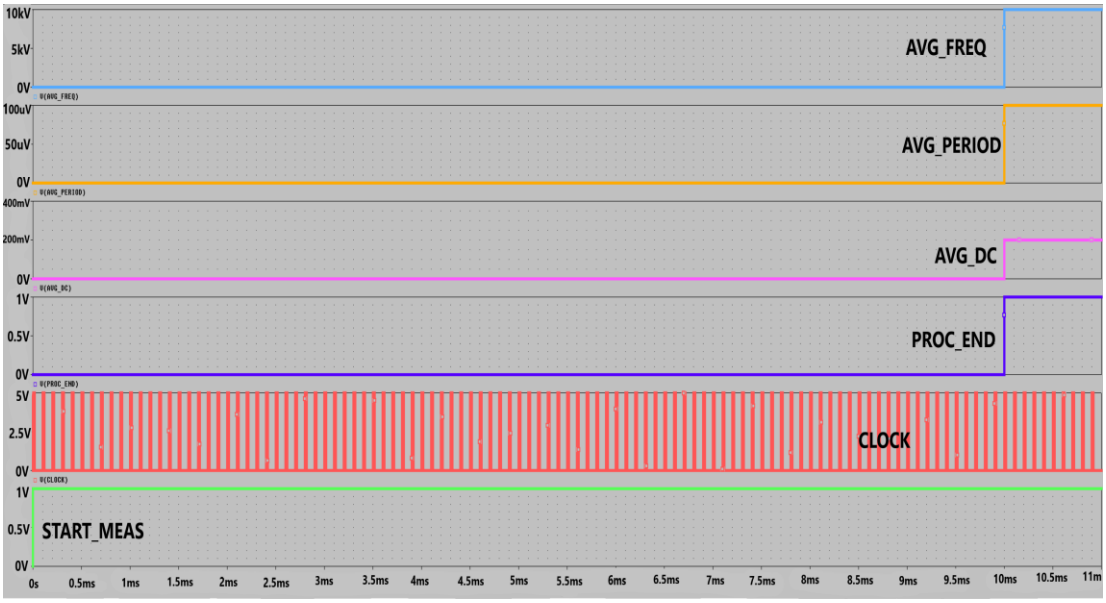


Figure 6.48 *OrCAD simulation waveforms for 10 kHz clock frequency, 0.2 duty cycle, and 100 sampled clock periods*

Conventional SPICE simulators only measure frequency and duty cycle post-simulation. Subchapter 6.5 introduced a novel real-time frequency measurement methodology for SPICE simulations, *detailed in author's original publication [143]*. The model measures and averages clock signal frequency, period, and duty cycle, featuring subcircuits for single clock period measurement, registers, a clocked addition module, and an up counter. Verified in OrCAD Capture, it provides high accuracy and fast simulation up to 1 GHz, ideal for clock synchronization in various applications.

6.6 Conclusions of chapter 6

Chapter 6 provided a detailed exploration of developing a comprehensive BMS model, focusing on accurately modeling internal digital circuits.

Subchapter 6.1 proposed a novel SPICE implementation of digital up-counters for BMS in ESS, showing expected behavior in all operations.

Subchapter 6.2 introduced an innovative down-counter SPICE model, demonstrating correct operation across the frequency spectrum.

Subchapter 6.3 presented a fully analog clock signal generator for SPICE-based simulators, exhibiting high quality and low error margins.

Subchapter 6.4 described an optimized slew rate control methodology for automotive LDO regulators, achieving high performance and precision.

Subchapter 6.5 introduced an enhanced frequency measurement methodology for SPICE-based simulators, showing high accuracy and rapid simulation times up to 1 GHz.

Chapter 7

SPICE Modeling and Simulation of a Passive BMS for Electric Vehicles

Subchapter 2.1 highlights that most BMS studies focus on physical design. SPICE simulation has been limited to specific components. Chapter 7 introduces a complete SPICE model for a passive BMS with four series-connected LiFePO4 cells, developed using OrCAD Capture.

Figure 7.2 shows the BMS block diagram.

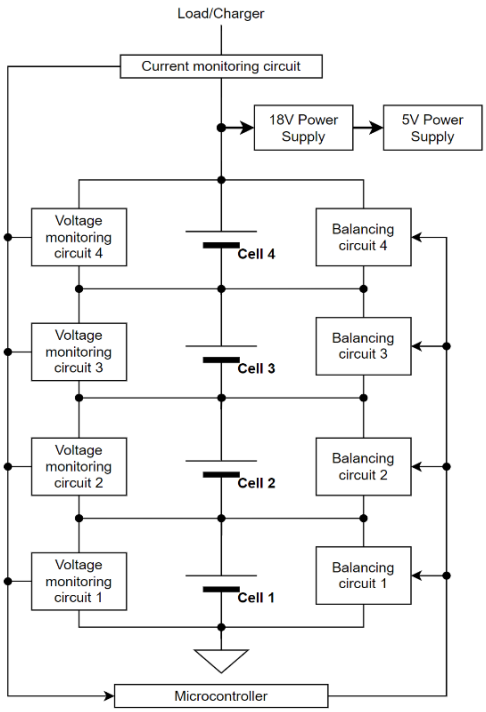


Figure 7.2 *Block diagram of the proposed BMS model*

7.1 Internal circuit modeling of the BMS

The BMS model balances four series-connected LiFePO4 cells. This section details the key internal circuits: cell voltage sensing, battery current sensing, passive cell balancing, power supply, and MCU.

Figure 7.3 shows the cell voltage sensing circuit.

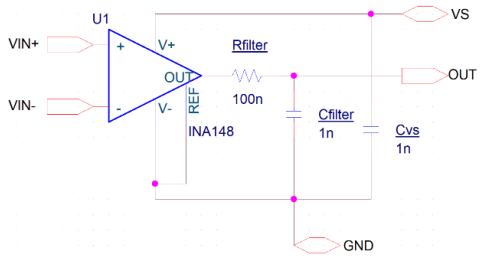


Figure 7.3 *Cell voltage sensing circuit model schematic*

Figure 7.7 shows the battery pack current sensing circuit.

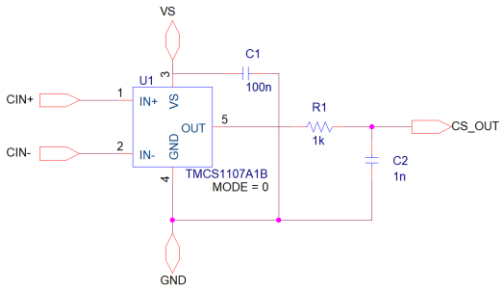


Figure 7.7 *Schematic of the battery pack current sensing circuit model*

Figure 7.10 shows the cell balancing circuit.

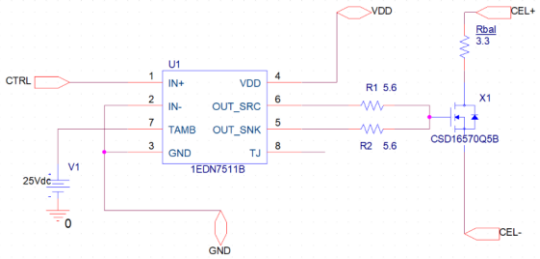


Figure 7.10 *Schematic of the cell balancing circuit model*

Figure 7.16 shows the power supply circuit.

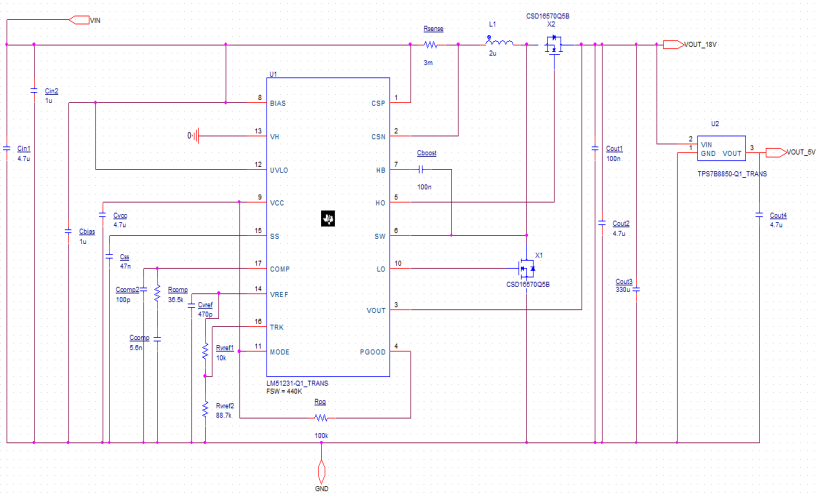


Figure 7.16 *Schematic of the power supply circuit model*

Figure 7.19 shows the MCU model interface.

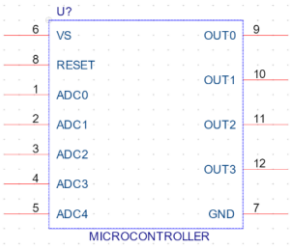


Figure 7.19 *MCU model interface*

7.2 Complete BMS model

The full BMS model integrates individual models from subchapter 7.1 and the LiFePO4 cell model from chapter 3. Figure 7.24 shows the detailed schematic of the final BMS model.

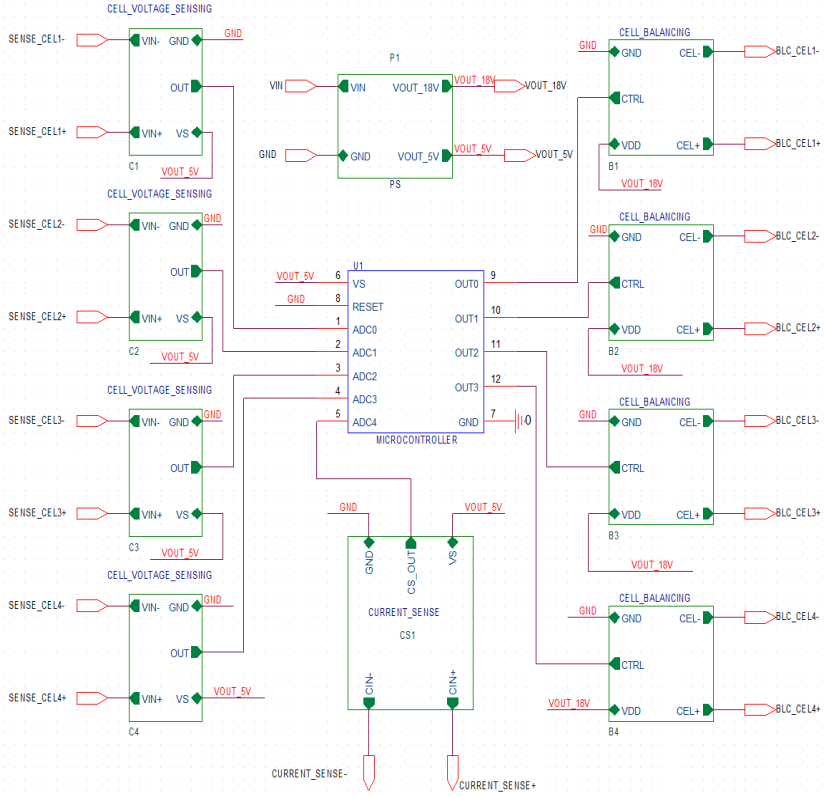


Figure 7.24 *Schematic of the complete BMS model*

7.3 Conclusions of chapter 7

Chapter 7 introduces a novel SPICE model for a BMS with four series-connected LiFePO4 cells. It measures cell voltages, charging/discharging currents, and performs passive balancing. *This work was previously detailed in author's original article [26]*.

The model was developed and tested in OrCAD Capture with high accuracy (voltage errors: 0.008%-0.04%, current error: 1.5%). This comprehensive BMS model is valuable for EVs, HEVs, ESSs, portable electronics, and photovoltaic systems.

Chapter 8

Hardware Development and Integration of a Passive BMS with Remote Monitoring Capabilities for Automotive Platforms

8.1 BMS design

This chapter details the hardwate design and implementation of a passive BMS for four series-connected LiFePO4 cells with the system architecture shown in Figure 8.1.

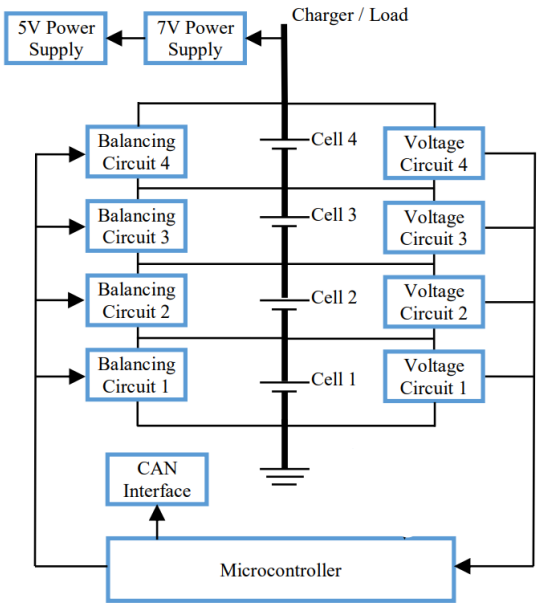


Figure 8.1 *System architecture of the proposed BMS*

Figures 8.13 and 8.14 show the passive BMS schematic, divided into analog and digital sections on separate Printed Circuit Boards (PCBs) for easy testing. Figure 8.13 (analog) includes the Buck converter and circuits for monitoring and balancing cell voltages. Figure 8.14 (digital) features the ATMEGA328P-AU MCU, cell voltage acquisition, indicator Light Emitting Diodes (LEDs), CAN monitoring (MCP2515, TJA1050T), and the 5 V LDO regulator.

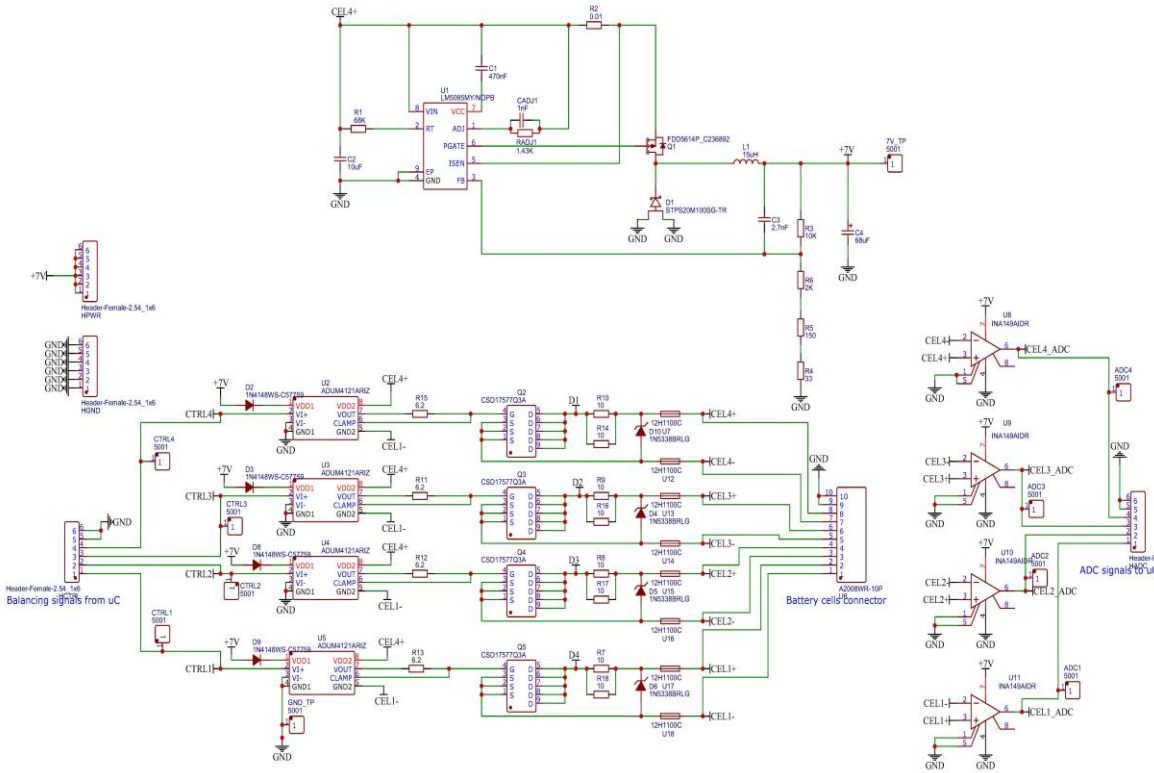


Figure 8.13 *Analog component of the BMS*

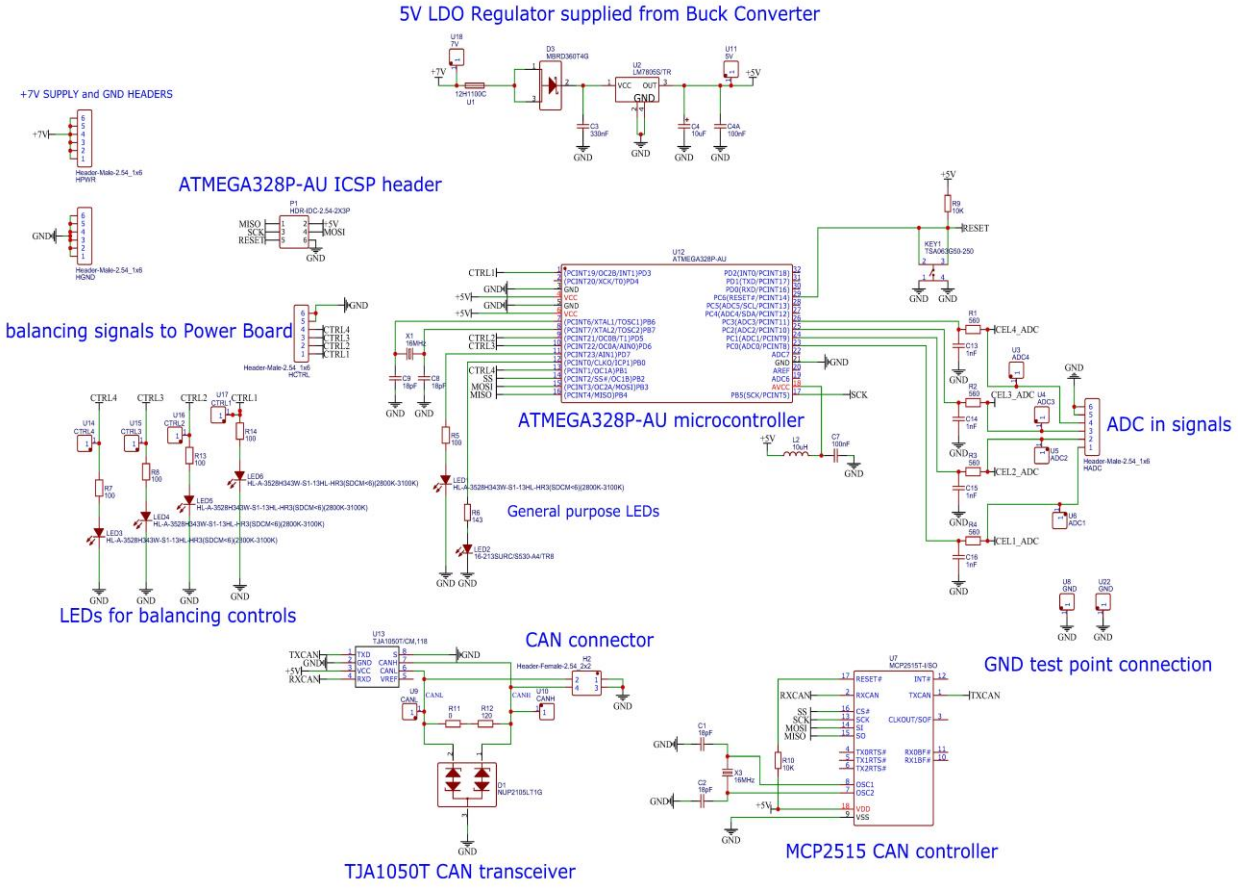
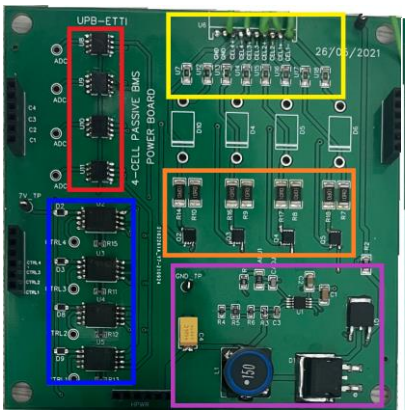


Figure 8.14 *Digital component of the BMS*

8.2 PCB assembly, integration and testing of the proposed BMS

The proposed BMS uses two PCBs for specific functionalities. The first PCB handles analog circuitry, including the Buck converter, cell balancing circuits, and cell voltage monitoring circuits. The second PCB is dedicated to digital circuitry, with the LDO regulator, ATMEGA328P-AU MCU, MCP2515 CAN controller, and TJA1050T CAN transceiver. This design allows for separate testing and faster verification.

Figure 8.16 shows the analog PCB, while Figure 8.17 shows the digital PCB.



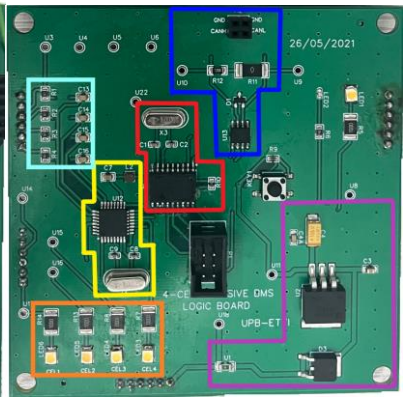


Figure 8.16 *Analog circuitry PCB* ***Figure 8.17*** *Digital circuitry PCB*

8.3 Results and comparative analysis

The proposed BMS achieves 0% - 0.03% voltage measurement error and 750 mA balancing current. Nizam et al. [186] had 0.367% - 0.535% error and 200 mA current. Xu et al. [187] achieved 0% - 0.166% voltage emasurement error. Ramelan et al. [188] obtained 7.5% error and 150 mA current. Canilang et al. [9] had 0.028% - 0.051% error and 110 mA current. The proposed BMS is faster and includes CAN remote monitoring.

8.4 Conclusions of chapter 8

This chapter presents a passive BMS for four series-connected CA180FA LiFePO4 cells, with remote monitoring via CAN for automotive applications. It uses passive balancing, featuring four cell voltage monitoring and balancing circuits. *This work was introduced in an author's previous original article [27].*

Verification shows a maximum voltage measurement error of 0.03% and balancing current error up to 1.19%, with effective cell balancing between 3.282 V and 3.322 V at 650-750 mA. It also adapts well to Li-ion batteries.

The BMS transmits cell voltages over CAN at 500 kbps and has a modular design for easy expansion.

Chapter 9

Conclusions

This thesis develops an advanced BMS for LiFePO4 batteries in automotive and ESS applications, focusing on SOC estimation and balancing to prevent degradation. The proposed passive BMS includes remote monitoring capabilities and offers superior results compared to existing methods.

For the first time, a full SPICE simulation model of a BMS is developed, providing a valuable tool for designers to test and optimize their designs without physical prototypes. The SPICE model simulates various operating conditions and evaluates performance in accuracy, reliability, and efficiency. It includes subcircuits like the LiFePO4 cell model, digital counter model, MOSFET RDSON model, PSRR model, frequency measurement for clock synchronization, slew-rate control, and clock signal generator.

This thesis significantly contributes to BMS design, simulation, implementation, and verification, offering a comprehensive understanding of the development cycle. The results improve the performance and longevity of LiFePO4 batteries, benefiting the automotive industry.

9.1 Obtained results

Chapter 1 highlights the importance of BMS in automotive and ESS applications, focusing on SOC estimation and balancing techniques for LiFePO4 batteries.

Chapter 2 reviews BMS literature, emphasizing the need for a complete SPICE model and favoring passive balancing for HEVs and EVs.

Chapter 3 introduces a SPICE model for a CALB CA180FA LiFePO4 cell, accurately capturing the OCV-SOC relationship.

Chapter 4 presents a new method for modeling MOSFET ON-state resistance, improving BMS power electronics simulations.

Chapter 5 enhances the PSRR response of automotive LDO models below 500 kHz, achieving significant accuracy improvements.

Chapter 6 develops a BMS model with digital circuit modeling, validated through extensive simulations.

Chapter 7 introduces a complete BMS SPICE model for four LiFePO4 cells, demonstrating high accuracy in voltage and current measurements.

Chapter 8 develops a passive BMS with CAN-based remote monitoring for automotive applications, achieving superior performance in voltage monitoring and balancing currents.

Chapter 9 concludes the thesis, summarizing results, contributions, and future perspectives.

9.2 Original contributions

The original contributions of the author are listed by chapters, as seen below.

Chapter 2:

- Identification of a significant gap in the literature: no complete, full-functionality BMS model has been proposed for SPICE or other simulation platforms.
- Highlighting the importance of developing a complete BMS SPICE model to streamline the BMS design process, making it more efficient, cost-effective, and reliable.
- Emphasizing the need for remote monitoring of battery parameters, which is a characteristic of modern BMS that has been overlooked in the literature.

Chapter 3:

- Development of a novel SPICE model for a CALB CA180FA LiFePO4 battery cell, enabling the creation and simulation of advanced ESSs, BMSs, and other battery-powered circuits.
- Model compatibility with all SPICE-based simulation software, including OrCAD Capture CIS, Pspice Allegro, TINA, SIMETRIX, and LTSpice, allowing designers to accurately model and analyze complex battery-based systems in their preferred simulator.

Chapter 4:

- Introduction of a novel and innovative approach to modeling ON-state resistance in MOSFET power switches, which enables precise control over the device's ON-state resistance by dynamically adjusting the gate-source voltage to achieve a specific target RDS_{ON} value.
- Development of a new CSD13380F3 MOSFET model that exhibits exceptional accuracy in replicating the datasheet RDS_{ON} characteristics. The new model outperforms the initial model in terms of accuracy, with a maximum error of 0.8% compared to 29.12% for the initial model.
- Addition of an independent temperature pin, enabling users to dynamically adjust the temperature during simulation, which allows for the emulation of the self-heating effect of the transistor.

Chapter 5:

- Introduction of a groundbreaking method for improving the PSSR of automotive LDO regulator models at low frequencies (below 500kHz), achieved by combining mathematical modeling techniques with circuit-level insights.
- Development of a new LDO model starting from an existing one, that exhibits excellent behavior at frequencies below 500 kHz, with a PSRR error of less than 7% compared with a PSRR error of 100% in case of the initial model.
- Identification of the need for accurate representation of the error amplifier's behavior to achieve accurate modeling across the entire frequency range.
-

Chapter 6:

- A novel SPICE implementation of digital up-counters for BMS, which behaves as expected during both normal operation and operation with clear output.
- An innovative approach to modeling a down-counter in SPICE, which operates correctly across the entire frequency spectrum.
- A new, fully analog approach for generating clock signals in SPICE-based simulators, which exhibits exceptional quality and low error margin across all simulators.
- An optimized slew rate control methodology tailored for automotive LDO regulators, which achieves high performance and precision in setting the slew rate with an error of 1.92% compared with an error of 50.52% achieved by the previous approach.
- An innovative frequency measurement methodology for clock synchronization in SPICE-based simulators, which demonstrates high accuracy and rapid simulation times for frequencies up to 1 GHz.

Chapter 7:

- Development for the first time in literature of a novel SPICE complete model of a BMS specifically designed for a battery pack consisting of four series-connected LiFePO4 cells, capable of measuring the voltage of each individual cell, as well as the charging and discharging currents, and performing passive balancing of the cells.
- Development of each block of the full BMS model: cell voltage sensing circuit model, cell balancing circuit model, current sensing circuit model, power supply circuit model, MCU model.
- Development of the balancing algorithm that activates the balancing circuit for any cell that has a voltage at least 25 mV higher than the most discharged cell.

Chapter 8:

- Design and physical implementation of a passive BMS with remote monitoring capabilities, tailored for the automotive domain, managing a battery comprising four CA180FA LiFePO4 cells connected in series, which achieves superior performance to other similar approaches in the literature in cell voltage monitoring accuracy and balancing speed.
- Use of a modular design that offers a key advantage, allowing for addition of multiple series-connected cells, thereby future-proofing the system.
- Use of a two-PCB design that enables separate testing and verification of each board.
- Achievement of 0.03% error in cell voltage monitoring and 1.19% error in balancing current.
- Presence of remote monitoring over the CAN interface using a standard CAN protocol at a data rate of 500 kpbs, characteristic that was not prioritized in BMSs until now.
- Demostration of BMS versatility by being able to also manage and balance Li-ion cells.

9.3 List of original publications

The author's original publications list comprises a total of 13 papers, with 2 of them published in ISI Q1 journals, 2 in ISI Q2 journals and 9 of them presented at scientific conferences between 2018-2024. The bibliography provides a complete list of these scientific papers. Notably, the content of all these previously mentioned works is closely related to the subject matter of this doctoral thesis.

During the PhD stage (2020-2025), the publication list comprises a total of 11 papers, with 2 of them published in ISI Q1 journals, 2 in ISI Q2 journals and 7 of them presented at scientific conferences.

I. Scientific Journal Papers

1. **Guran, Ionuț-Constantin**, Adriana Florescu, and Lucian Andrei Perișoară, "Optimized Power Supply Rejection Ratio Modeling Technique for Simulation of Automotive Low-Dropout Linear Voltage Regulators", *Mathematics* 10, no. 7: 1150. https://doi.org/10.3390/math10071150, Categories/Classification: Research Areas Mathematics, Citation Topics 4. Electrical Engineering, Electronics & Computer Science, 2022, **WOS:000781254000001** ***(ISI Q1 journal, Journal Impact Factor 2023 = 2,3) [93]***
2. **Guran, Ionuț-Constantin**, Adriana Florescu, and Lucian Andrei Perișoară, "A Novel ON-State Resistance Modeling Technique for MOSFET Power Switches", *Mathematics* 11, no. 1: 72. https://doi.org/10.3390/math11010072, Categories/Classification: Research Areas Mathematics, Citation Topics 4. Electrical Engineering, Electronics & Computer Science, 2023, **WOS:000909663000001** ***(ISI Q1 journal, Journal Impact Factor 2023 = 2,3) [68]***
3. **I. -C. Guran**, A. Florescu and L. A. Perisoara, "A Novel Frequency Measurement Methodology for Clock Synchronization in SPICE-Based Simulators" in *IEEE Access*, vol. 11, pp. 117030-117039, 2023, doi: 10.1109/ACCESS.2023.3324883, **WOS:001096961500001*****(ISI Q2 journal, Journal Impact Factor 2023 = 3,4) [143]***
4. **I. -C. Guran**, A. Florescu and L. A. Perișoară, "SPICE Model of a Passive Battery Management System" in *IEEE Access*, vol. 12, pp. 4000-4014, 2024, doi: 10.1109/ACCESS.2023.3349186, **WOS:001140270200001** ***(ISI Q2 journal, Journal Impact 2023 = 3,4) [26]***

II. Scientific Conference Papers

a) Original publications *before* the doctoral stage (2020-2025)

1. L. A. Perișoară, ***I. C. Guran*** and D. C. Costache, "A Passive Battery Management System for Fast Balancing of Four LiFePO4 Cells", *2018 IEEE 24th International Symposium for Design and Technology in Electronic Packaging (SIITME)*, Iasi, Romania, 2018, pp. 390-393, doi: 10.1109/SIITME.2018.8599258, **WOS:000466960400083** ***(ISI conference) [101]***
2. L. A. Perișoară, D. C. Costache, **I. C. Guran**, Ș. George Roșu and A. Florescu, "Active Balancing for Efficient Management of a 4S1P LiFePO4 Battery Pack", *2019 11th International Symposium on Advanced Topics in Electrical Engineering (ATEE)*, Bucharest, Romania, 2019, pp. 1-6, doi: 10.1109/ATEE.2019.8724917, **WOS:000475904500074** ***(ISI conference) [98]***

b) Original publications *during* the doctoral stage (2020-2025)

1. **Ionuț-Constantin Guran** and Lucian-Andrei Perișoară "MPPT solar charge controller for automotive industry", Proc. SPIE 11718, *2020 Advanced Topics in Optoelectronics, Microelectronics and Nanotechnologies X, 117182Q (31 December 2020)*; https://doi.org/10.1117/12.2572100, **WOS:000641147900097** ***(ISI conference) [189]***
2. **I. C. Guran**, L. Andrei Perișoară and A. Florescu, "SPICE Model Implementation for LiFePO4 Cell", *2020 International Symposium on Fundamentals of Electrical Engineering (ISFEE)*, Bucharest, Romania, 2020, pp. 1-4, doi: 10.1109/ISFEE51261.2020.9756177, **WOS:000812321500046000466960400083** ***(ISI conference) [30]***
3. **I. C. Guran**, L. A. Perișoară, A. Florescu and D. I. Săcăleanu, "4-Cell Passive Battery Management System for Automotive Applications", *2021 IEEE 27th International Symposium for Design and Technology in Electronic Packaging (SIITME)*, Timisoara, Romania, 2021, pp. 338-341, doi: 10.1109/SIITME53254.2021.9663604, **WOS:000786441900080** ***(ISI conference) [20]***
4. **I. -C. Guran**, A. Florescu, L. -A. Perişoară, M. S. Teodorescu and I. B. Bacîş, "SPICE Implementation of Digital Counters for Battery Management Systems Used in Energy Storage Systems", *2022 14th International Conference on Electronics, Computers and Artificial Intelligence (ECAI)*, Ploiesti, Romania, 2022, pp. 1-4, **doi: 10.1109/ECAI54874.2022.9847485** ***(BDI conference indexed IEEE) [119]***
5. **I. -C. Guran**, A. Florescu, L. -A. Perişoară, A. Vasile and C. -D. Oancea, "Fully Analog Clock Signal Generator for SPICE based simulators", *2022 14th International Conference on Electronics, Computers and Artificial Intelligence (ECAI)*, Ploiesti, Romania, 2022, pp. 1-4, **doi: 10.1109/ECAI54874.2022.9847455** ***(BDI conference indexed IEEE) [121]***
6. **I. -C. Guran**, A. Florescu and L. -A. Perişoară, "Optimized Slew Rate Control Technique for Automotive Low-Dropout Linear Voltage Regulators Simulation Models", *2022 14th International Conference on Electronics, Computers and Artificial Intelligence (ECAI)*, Ploiesti, Romania, 2022, pp. 1-4, **doi: 10.1109/ECAI54874.2022.9847436** ***(BDI conference indexed IEEE) [142]***
7. **I. -C. Guran**, A. Florescu, L. A. Perișoară, M. Ș. Teodorescu, I. B. Bacîș and A. Vasile, "Advanced Down-Counting Operation in SPICE", *2023 13th International Symposium on Advanced Topics in Electrical Engineering (ATEE)*, Bucharest, Romania, 2023, pp. 1-4, **doi: 10.1109/ATEE58038.2023.10108172** ***(BDI conference indexed IEEE) [120]***

9.4 Perspectives for further developments

Future developments include creating a SPICE model for a Finite State Machine (FSM) to enhance the MCU model's realism in the BMS.

The LiFePO4 cell model will be refined to include self-heating effects and temperature fluctuations for improved accuracy.

The balancing algorithm will be optimized to use SOC estimation via the Coulomb counting method, increasing precision and reliability.

The BMS design will also be enhanced to support current and temperature sensing and scalability for up to 16 LiFePO4 cells, aligning with the automotive industry's shift to 48 V systems.

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